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PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of :
KHANDROS et al. :
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Application No. 09/656,690 :
:
Filed: September 7, 2000 :
:
For: SEMICONDUCTOR CHIP :
ASSEMBLIES, METHODS OF :
MAKING SAME AND :
COMPONENTS FOR SAME X

Group Art Unit: 2814

Examiner: D. Graybill

Date: September 20, 2001

9 Response
J Mackey
9-26-01

Commissioner for Patents
Washington, D.C. 20231

RESPONSE

The present communication is responsive to the Official Action mailed August 20, 2001. Said Official Action set forth a term of "one-month or thirty days, whichever is longer" from the mailing date. Accordingly, the present response is timely filed with certificate of mailing on or before September 20, 2001.

The Official Action sets forth a requirement that the Applicant "specifically apply each limitation or element of each of the copied claims to the disclosure of the application." The table set forth below is presented in response to that requirement. A few passages quoted in the table include matter that had previously been amended. Matter previously inserted by amendment in the application is enclosed in brackets "{}." The amendatory matter does not affect the meaning of the quoted passages or of the

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specification as a whole. In addition, the claims have been subdivided, in claims 1 and 7, to break out individual features. These subdivisions are denoted by paragraph numbers as, for example, <1(a)1>.

It is noted that the Official Action did not require Applicant to set forth an exhaustive list of all of the disclosure in the application that supports the various limitations of the claims and accordingly the present submission should not be taken as such an exhaustive list.

Claims	Disclosure of the Application
1. A method of assembling a plurality of semiconductor chips, comprising the steps of:	
<1(a)1> (a) providing a portion of a semiconductor wafer containing the plurality of chips thereon,	"{As illustrated in Fig. 31,} chips {928} may be provided in the form of a wafer {930} incorporating a plurality of chips…" Page 30, lines 32-34. "A wafer incorporating a plurality of chips may be assembled...." Page 31, lines 11-13.
<1(a)2> each of the plurality of chips having a contact pattern area including a pattern of contacts on a surface of the chip;	"...a semiconductor chip having a front surface with a plurality of contacts disposed in a pattern on the front surface. The pattern of contacts on the front surface encompasses an area, referred to herein as the 'contact pattern area' on the front surface." Page 7, lines 21-26. One such chip 28 with contacts 40 on its front surface is

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	depicted in Figs. 4 and Figs. 7-9. "As best seen in FIG. 4, the contacts 40 on chip 28 (each symbolized by a dot in FIG. 4) are disposed in a pattern on the front surface of chip 28. Contacts 40 cooperatively encompass a contact pattern area 62 on the front face of chip 28." Page 21, lines 6-10. "a chip having a front surface including a central region and a peripheral region surrounding the central region, the chip having a plurality of peripheral contacts disposed in the peripheral region of the front surface." Page 9, lines" 19-23 In Figs 11-13, "The chip 820 also has a plurality of peripheral contacts 830 arranged in rows 832, there being one such row adjacent each edge 828 of the chip." Page 32, lines 12-14.
<1(b)1> (b) assembling a respective section of a dielectric interposer to each respective one of the plurality of chips individually, without detaching the	"Individual, separate, interposers {924} may be positioned on the individual chips constituting wafer {930} and the interposers may be assembled to the chips... After the interposers are secured to the chips, and desirably after the junctures between the leads of each interposer and the contacts of each chip are

Claims	Disclosure of the Application
plurality of chips from the portion of the semiconductor wafer,	encapsulated, the individual chips are separated from the wafer and from one another..." Page 30, line 34-Page 31, line 5. To perform this sequence of operations, in which the chips are severed "after" assembly of the interposers to the chips and after subsequent operations, the step of assembling the interposers to the chips necessarily is performed without detaching the chips from the wafer.
<1(b)2> each section of interposer having a plurality of bonding pads near an outer periphery of the section,	"Bonding terminals 852 are arranged in rows 854 adjacent the edges of the interposer." Page 34, lines 9-10 and Fig. 13. The terminals 48 depicted in Fig. 9 include bonding pads which are connected to the contacts by wire bonds. Page 29, lines 4-7. In this embodiment, at least some of the terminals, and the bonding pads incorporated in those terminals, are depicted in Fig. 9 as disposed adjacent the periphery of the interposer or "section". "...the outermost terminals 48 desirably lie within or close to the boundary B of the contact array area 62" See Fig. 4 and page 21, lines 6-page 22, line 11.
<1(b)3>	In Fig. 13, "...the interposer 836

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such that each bonding pad lies near the contact pattern area of the corresponding one of the plurality of chips;	with the ...bonding terminals 852 thereon is positioned on chip 820...so that the edges 846 of the interposer are disposed inwardly of the rows 832 of peripheral contacts 830 on the chip....The arrangement of the bonding terminals 852 in rows parallel to and adjacent to the rows of peripheral contacts 830 on the chip..." Page 34, lines 15-26. Further, the specification teaches that when an interposer is assembled to overlie the front or contact-bearing surface of a chip (as in Figs 13 and 9) "[a]t least some of these terminals, and preferably most or all of these terminals, are disposed within the area of the interposer overlying the contact pattern area on the chip." Page 7, line 37-Page 8, line 3. In conformity with these teachings, the terminals (and the bonding pads) of Fig. 9 overlie the contact pattern area of the chip associated with that interposer and hence the bonding pads are disposed "near" the contact pattern area.
<1(c)> (c) wire bonding each bonding pad to a respective one of the contacts on the front	"The flexible leads may be formed integrally with the terminals on the interposer, or else may be separately formed fine wires." Page 8, lines 33-35.

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surface of the corresponding one of the plurality of chips;	"...the peripheral contact leads may be formed after the interposer is applied to the chip, as in a wire-bonding step in which a fine wire is dispensed and formed into a lead connecting the contact and terminal." Page 12, lines 25-29. "Bonding terminals 852 are electrically connected to contacts 830 on the chip by a conventional wire bonding operation." Page 34, lines 21-23 and Fig. 13. The bonding pads associated with the terminals depicted in Fig. 9 are connected by bonding "pieces of fine wire" to the contacts to provide leads 50'.. Page 29, lines 4-7.
<1(d)> (d) applying an encapsulant to encapsulate the wires on each of the plurality of chips; and	"In the next stage of the process, a...encapsulant ...is applied over the interposer and chip and over bonding wires 856." Page 25,lines 1-5. "The subassembly illustrated in Fig. 9 may be further provided with an encapsulant (not shown) in the form of a layer ...covering the leads 50'." Page 29, lines 15-18. After the terminals and contacts are connected to one another, and before the individual chips of the wafer are severed from one another, the connections between the leads and contacts are encapsulated. Page 31,

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	lines 1-8.
<1(e)> (e) cutting the encapsulated chips from the semiconductor wafer.	The chips are severed from one another utilizing dicing equipment "desirably after the junctures between the leads of each interposer and the contacts of each chip are encapsulated". Page 31, lines 4-8.
2. A method according to claim 1, wherein step (c) includes bonding one end of each wire to a respective bonding pad using one of the group consisting of micro resistant welding and ultrasonic bonding.	As shown in Fig. 9, fine wires 50' are attached to the bonding pads associated with terminals 48 on the interposer and the contacts 40 on the chip to provide the leads. Page 26, lines 1-7. Also, "Bonding terminals 852 are electrically connected to contacts 830 on the chip by a conventional wire bonding operation." Page 32 lines 21-23 and Fig. 13. The tool utilized in bonding may comprise a thermal, thermosonic, ultrasonic, compression tool, or other tool utilized in conventional tape automated bonding or wire bonding. Page 26, lines 17-25.
3. A method according to claim 1, wherein step (b) includes providing an elastomer between each of the plurality of chips and the respective interposer on the chip.	"Most preferably, a compliant layer is disposed between said terminals and said chip ... The complaint layer may be incorporated in the sheetlike element, or formed separately therefrom." Page 5,line 34-Page 6, line 2. In the embodiment shown in Fig. 13, the compliant layer 840 of the

Claims	Disclosure of the Application
	interposer comprises an elastomeric material. Page 32, line 27-page 33, line 3. The compliant layer 840 is disposed between top layer 838 of the interposer and chip 820. See Fig. 13. A compliant layer formed from a "elastomer" is positioned on the top surface of the chip before the top layer 838 is assembled to the chip. Page 41, lines 19-35. The use of a compliant layer in the "interposer 42" of Fig. 9 is mentioned at Page 19, lines 14-16, where the same element is described with different leads.
4. A method according to claim 1, wherein the portion of the semiconductor wafer includes the whole semiconductor wafer.	"Chips may be provided in the form of a wafer incorporating a plurality of chips..." Page 30, lines 32-34. "A wafer incorporating a plurality of chips may be assembled...." Page 31, lines 11-13.
5. A method according to claim 1, wherein one end of each wire is bonded to a respective bonding pad of the interposer using ultrasonic bonding, and the other end of each wire is bonded to a respective	See claim 2.

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contact of the chip using ultrasonic bonding.	
6. A method according to claim 1, wherein step (c) includes bonding one of the wires that is oriented at an angle substantially less than 90 degrees from any side of the section of interposer having the bonding pad to which the one wire is bonded.	The "interposer 836" of Fig. 13 has "edges 846". Page 33, lines 9-10. The wires of Fig. 13 extend across the edges. Page 34, lines 9-37. FIG. 13 shows one bonding wire 856 (at the lower left hand corner of the drawing) extending at an angle to edge 846 different from the angles between the other bonding wires and the same edge. Manifestly, at least one bonding wire extends at an angle other than 90° to the particular edge 846 seen in the fragmentary of FIG. 13. The same interposer 836 is also illustrated in full plan view in FIG. 12. The interposer 836 is rectangular and hence the various edges 846 of the interposer lie at right angles to one another. A bonding wire which extends at an angle of other than 90° to the single edge depicted in FIG. 13 is also at an angle of other than 90° to any edge of the interposer or "section"
7. A method of assembling a plurality of semiconductor chips, comprising the steps of:	

Claims	Disclosure of the Application
<7(a)1> (a) providing a portion of a semiconductor wafer containing the plurality of chips thereon,	"{As illustrated in Fig. 31, } chips {928} may be provided in the form of a wafer {930} incorporating a plurality of chips…" Page 30, lines 32-34. "A wafer incorporating a plurality of chips may be assembled to a sheet incorporating a plurality of interposers." Page 31, lines 11-13.
<7(a)2> each of the plurality of chips having a contact pattern area including a pattern of contacts on a surface of the chip;	"...a semiconductor chip having a front surface with a plurality of contacts disposed in a pattern on the front surface. The pattern of contacts on the front surface encompasses an area, referred to herein as the 'contact pattern area' on the front surface." Page 7, lines 21-26. One such chip 28 with contacts 40 on its front surface is depicted in Figs. 4 and Figs. 7-9. "As best seen in FIG. 4, the contacts 40 on chip 28 (each symbolized by a dot in FIG. 4) are disposed in a pattern on the front surface of chip 28. Contacts 40 cooperatively encompass a contact pattern area 62 on the front face of chip 28." Page 21, lines 6-10. "a chip having a front surface including a central region and a peripheral region surrounding the central region, the chip having a plurality of peripheral

Claims	Disclosure of the Application
	contacts disposed in the peripheral region of the front surface." Page 9, lines" 9-23 In Figs 11-13, "The chip 820 also has a plurality of peripheral contacts 830 arranged in rows 832, there being one such row adjacent each edge 828 of the chip." Page 32, lines 12-14.
<7(b)1> (b) assembling a sheet including a plurality of interposers to said portion of said semiconductor wafer so that each said interposer is assembled to an associated one of the plurality of chips, without detaching the plurality of chips from the portion of the semiconductor wafer,	Alternatively,{as illustrated in Figure 32,} a wafer {950} incorporating a plurality of chips may be assembled to a sheet{952} incorporating a plurality of interposers {954}. Again, the contacts on each chip are secured to the terminals and leads of one individual interposer overlying the particular chip. The wafer {950} and the sheet {952} are severed after this operation, and desirably after encapsulating the leads, so as to provide individual subassemblies..." Page 31, lines 12-19. To perform this sequence of operations, in which the chips are severed from the wafer "after" assembly of the interposers to the chips and after subsequent operations, the step of assembling the sheet of interposers to the wafer necessarily is performed without detaching the chips from the wafer.

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<7(b)2> each said interposer having a plurality of bonding terminals near an outer periphery of the interposer,	"Bonding terminals 852 are arranged in rows 854 adjacent the edges of the interposer." Page 34, lines 9-10 and Fig. 13. Additionally, the terminals 48 depicted in Fig. 9 include bonding pads which are connected to the contacts by wire bonds. Page 29, lines 4-7. In this embodiment, at least some of the terminals, and the bonding pads incorporated in those terminals, are depicted in Fig. 9 as disposed adjacent the periphery of the interposer or "section". "...the outermost terminals 48 desirably lie within or close to the boundary B of the contact array area 62" See Fig. 4 and page 21, lines 6-page 22, line 11.
<7(b)3> such that each bonding terminal of each said interposer lies near the contacts of the one of the plurality of chips associated with that interposer;	In the embodiment of Fig. 13, "...the interposer 836 with the ...bonding terminals 852 thereon is positioned on chip 820...so that the edges 846 of the interposer are disposed inwardly of the rows 832 of peripheral contacts 830 on the chip....The arrangement of the bonding terminals 852 in rows parallel to and adjacent to the rows of peripheral contacts 830 on the chip..." Page 34, lines 15-26.

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	Further, the specification teaches that when an interposer is assembled to overlie the front or contact-bearing surface of a chip (as in Figs 13 and 9) "[a]t least some of these terminals, and preferably most or all of these terminals, are disposed within the area of the interposer overlying the contact pattern area on the chip." Page 7, line 37-Page 8, line 3. In conformity with these teachings, the terminals (and the bonding pads) of Fig. 9 overlie the contact pattern area of the chip associated with that interposer and hence the bonding pads are disposed "near" the contact pattern area.
<7(c)> (c) wire bonding each bonding terminal to a respective one of the contacts on the front surface of the corresponding one of the plurality of chips;	"The flexible leads may be formed integrally with the terminals on the interposer, or else may be separately formed fine wires." Page 8, lines 33-35. "...the peripheral contact leads may be formed after the interposer is applied to the chip, as in a wire-bonding step in which a fine wire is dispensed and formed into a lead connecting the contact and terminal." Page 12, lines 25-29 "Bonding terminals 852 are electrically connected to contacts 830 on the chip by a conventional

Claims	Disclosure of the Application
	wire bonding operation." Page 34, lines 21-23 and Fig. 13. The bonding pads associated with the terminals depicted in Fig. 9 are connected by bonding "pieces of fine wire" to the to the contacts to provide leads 50'.. Page 29, lines 4-7.
<7(d)> (d) applying an encapsulant to encapsulate the wires on each of the plurality of chips; and	"In the next stage of the process, a...encapsulant ...is applied over the interposer and chip and over bonding wires 856." Page 25,lines 1-5. "The subassembly illustrated in Fig. 9 may be further provided with an encapsulant (not shown) in the form of a layer ...covering the leads 50'." Page 29, lines 15-18. After the terminals and contacts are connected to one another, and before the individual chips of the wafer are severed from one another, the leads are encapsulated. Page 31, lines 17-18.
<7(e)> (e) cutting the encapsulated chips from the semiconductor wafer.	The wafer and the sheet are "severed...desirably after encapsulating..." to provide "individual subassemblies each including a chip and an interposer." Page 31, lines 17-19.
8. A method according to claim 7, wherein step (c)	See claim 2.

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includes bonding one end of each wire to a respective bonding terminal using ultrasonic bonding.	
9. A method according to claim 7, wherein step (b) includes providing an elastomer between each of the plurality of chips and the interposer associated with that chip.	See claim 3.
10. A method according to claim 7, wherein the portion of the semiconductor wafer includes the whole semiconductor wafer.	See claim 4.
11. A method according to claim 7, wherein one end of each wire is bonded to a respective bonding terminal of the interposer using ultrasonic bonding, and the other end of each wire is bonded to a respective contact	See claim 8.

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of the chip using ultrasonic bonding.	
12. A method according to claim 7, wherein step (c) includes bonding one of the wires that is oriented at an angle substantially less than 90 degrees from any side of the section of interposer having the bonding terminal to which the one wire is bonded.	See claim 6.
13. A method of assembling a plurality of semiconductor chips, comprising the steps of:	
(a) providing a semiconductor wafer containing the plurality of chips thereon,	See <7(a)1>
each of the plurality of chips having a contact pattern area including a pattern of contacts on a surface of the chip;	See <7(a)2>
(b) assembling a	See <7(b)1>.

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sheet including a plurality of interposers to said semiconductor wafer so that each said interposer is assembled to an associated one of the plurality of chips, without detaching the plurality of chips from the semiconductor wafer,	
each said interposer having a plurality of bonding terminals near an outer periphery of the interposer,	See <7(b)2>
such that each bonding terminal of each said interposer lies near the contacts of the one of the plurality of chips associated with that interposer;	See <7(b)3>
(c) wire bonding each bonding terminal to a respective one of the contacts on the front surface of the corresponding one of the plurality of	See <7(c)>.

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chips;	
(d) applying an encapsulant to encapsulate the wires on each of the plurality of chips; and	See <7(d)>.
(e) cutting the encapsulated chips from the semiconductor wafer.	See <7(e)>.
14. A method according to claim 13, wherein step (c) includes bonding one end of each wire to a respective bonding terminal using ultrasonic bonding.	See claim 2.
15. A method according to claim 13, wherein step (b) includes providing an elastomer between each of the plurality of chips and the interposer associated with that chip.	See claim 3.
16. A method according to claim 13, wherein one end of each wire is bonded to	See claim 8.

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a respective bonding terminal of the interpose using ultrasonic bonding, and the other end of each wire is bonded to a respective contact of the chip using ultrasonic bonding.	
17. A method according to claim 13, wherein step (c) includes bonding one of the wires that is oriented at an angle substantially less than 90 degrees from any side of the section of interposer having the bonding terminal to which the one wire is bonded.	See claim 6.
18. A method of assembling a plurality of semiconductor chips, comprising the steps of:	
(a) providing a portion of a semiconductor wafer containing the plurality of chips	See <1(a)1>.

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thereon,	
each of the plurality of chips having a contact pattern area including a pattern of contacts on a surface of the chip;	See <1(a)2>
(b) assembling a respective section of a dielectric interposer to each respective one of the plurality of chips individually, without detaching the plurality of chips from the portion of the semiconductor wafer,	See <1(b)1>.
each section of interposer having a plurality of bonding pads near an outer periphery of the section,	See <1(b)2>.
such that each bonding pad lies near the contact pattern area of the corresponding one of the plurality of chips;	See <1(b)3>.
(c) wire bonding each	See <1(c)>

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bonding pad to a respective one of the contacts on the front surface of the corresponding one of the plurality of chip whereby wires extend from the bonding pads to the contacts;	
(d) applying an encapsulant to encapsulate the wires on each of the plurality of chips; and	See <1(d)>
(e) cutting the encapsulated chips from the semiconductor wafer.	See <1(e)>
19. A method according to claim 18, wherein step (c) includes bonding one end of each one of said wires to a respective bonding pad using one of the group consisting of micro resistant welding and ultrasonic bonding.	See claim 2.
20. A method according to claim 18,	See claim 3.

Claims	Disclosure of the Application
wherein step (b) includes providing an elastomer between each of the plurality of chips and the respective interposer on the chip.	
21. A method according to claim 18, wherein the portion of the semiconductor wafer includes the whole semiconductor wafer.	See claim 4.
22. A method according to claim 18, wherein one end of each wire is bonded to a respective bonding pad of the interposer using ultrasonic bonding, and the other end of each wire is bonded to a respective contact of the chip using ultrasonic bonding.	See claim 5.
23. A method according to claim 18, wherein each said section of the interposer has edges	See claim 6.

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and wherein step (c) includes bonding one of the wires extending from a bonding pad of one said section so that said one of the wires is oriented at an angle other than 90 degrees from any edge of said one said section.	
24. A method of assembling a plurality of semiconductor chips, comprising the steps of:	
(a) providing a portion of a semiconductor wafer containing the plurality of chips thereon,	See <7(a)1>.
each of the plurality of chips having a contact pattern area including a pattern of contacts on a surface of the chip;	See <7(a)2>
(b) assembling a sheet including a plurality of interposers to said	See <7(b)1>.

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portion of said semiconductor wafer so that each said interposer is assembled to an associated one of the plurality of chips, without detaching the plurality of chips from the portion of the semiconductor wafer,	
each said interposer having a plurality of bonding terminals near an outer periphery of the interposer,	See <7(b)2>
such that each bonding terminal of each said interposer lies near the contacts of the one of the plurality of chips associated with that interposer;	See <7(b)3>
(c) wire bonding each bonding terminal to a respective one of the contacts on the front surface of the corresponding one of the plurality of chips whereby wires extend	See <7(c)>.

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from the bonding pads to the contacts;	
(d) applying an encapsulant to encapsulate the wires on each of the plurality of chips; and	See <7(d)>.
(e) cutting the encapsulated chips from the semiconductor wafer.	See <7(e)>.
25. A method according to claim 24, wherein step (c) includes bonding one end of each one of said wires to a respective bonding terminal using ultrasonic bonding.	See claim 2.
26. A method according to claim 24, wherein step (b) includes providing an elastomer between each of the plurality of chips and the interposer associated with that chip.	See claim 3.
27. A method according to claim 24,	See claim 4.

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wherein the portion of the semiconductor wafer includes the whole semiconductor wafer.	
28. A method according to claim 24, wherein one end of each wire is bonded to a respective bonding terminal of the interposer using ultrasonic bonding, and the other end of each wire is bonded to a respective contact of the chip using ultrasonic bonding.	See claim 5.
29. A method according to claim 24, wherein each said section of the interposer has edges and wherein step (c) includes bonding one of the wires extending from a bonding pad of one said section so that said one of the wires is oriented at an angle other than 90 degrees from any edge	See claim 6.

Claims	Disclosure of the Application
of said one said section.	
30. A method of assembling a plurality of semiconductor chips, comprising the steps of:	
(a) providing a semiconductor wafer containing the plurality of chips thereon,	See <7(a)1>.
each of the plurality of chips having a contact pattern area including a pattern of contacts on a surface of the chip;	See <7(a)2>
(b) assembling a sheet including a plurality of interposers to said semiconductor wafer so that each said interposer is assembled to an associated one of the plurality of chips, without detaching the plurality of chips from the semiconductor wafer,	See <7 (b)1>.

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each said interposer having a plurality of bonding terminals near an outer periphery of the interposer,	See <7(b)2>
such that each bonding terminal of each said interposer lies near the contacts of the one of the plurality of chips associated with that interposer;	See <7(b)3>
(c) wire bonding each bonding terminal to a respective one of the contacts on the front surface of the corresponding one of the plurality of chips whereby wires extend from the bonding pads to the contacts;	See <7(c)>.
(d) applying an encapsulant to encapsulate the wires on each of the plurality of chips; and	See <7(d)>.
(e) cutting the encapsulated chips from the semiconductor wafer.	See <7(e)>.

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31. A method according to claim 30, wherein step (c) includes bonding one end of each one of said wires to a respective bonding terminal using ultrasonic bonding.	See claim 2.
32. A method according to claim 30, wherein step (b) includes providing an elastomer between each of the plurality of chips and the interposer associated with that chip.	See claim 3.
33. A method according to claim 30, wherein one end of each wire is bonded to a respective bonding terminal of the interpose using ultrasonic bonding, and the other end of each wire is bonded to a respective contact of the chip using ultrasonic bonding.	See claim 5.

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34. A method according to claim 30, wherein each said section of the interposer has edges and wherein step (c) includes bonding one of the wires extending from a bonding pad of one said section so that said one of the wires is oriented at an angle other than 90 degrees from any edge of said one said section.	See claim 6.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

Respectfully submitted,

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